## Ultra Low Capacitance ESD Protection Array

## DESCRIPTION

SLESD0504F is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to protection for high-speed data interfaces. With typical capacitance of 0.20pF (I/O to I/O) only, SLESD0504F is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4(±15KV air, ±8KV contact discharge), IEC61000-4-4 (electrical fast transient-EFT) (40A, 5/50ns),very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

SLESD0504F uses small SOT-363 package. Each SLESD0504F device can protect four high-speed data lines one Vcc line. The combined features of ultra-low capacitance, small size and high ESD robustness make SLESD0504F ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the SLESD0504F guarantees a minimum stress on the protected IC.

## FEATURES

✧Transient protection for high-speed data lines
IEC 61000-4-2(ESD) ±25KV(Air)
±20KV(Contact)
IEC 61000-4-4(EFT)40A(5/50ns)
Cable Discharge Event(CDE)
✧Package optimized for high-speed lines
✧Small package(2.1mm*2.3mm*1.0mm)
✧Protects four data lines and one Vcc line
✧Low capacitance: 0.20pF (I/O to I/O)
✧Low leakage current
✧Low clamping voltage
✧Each I/O pin can withstand over 1000 ESD strikes for ±8KV contact discharge

## MACHANICAL DATA

✧SOT-363 package
✧Flammability Rating: UL 94V-0
✧Terminal: Matte tin plated.
✧Packaging: Tape and Reel
✧High temperature soldering guaranted:260℃/10s
✧Reel size: 7 inch

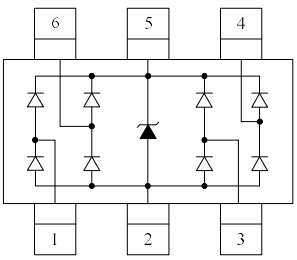
## ORDERING INFORMATION

✧Device: SLESD0504F
✧Package: SOT-363
✧Marking: F54
✧Material: Halogen free
✧Packing: Tape & Reel
✧Quantity per reel: 3,000pcs

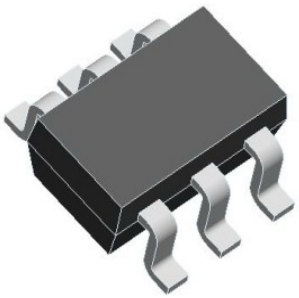
## APPLICATIONS

✧Serial ATA
✧MDDI Ports
✧USB 2.0/3.0 Power and Data Line Protection
✧Display Ports
✧High Definition Multi-Media Interface (HDMI)
✧Digital Visual Interface (DVI)

## PIN CONFIGURATION




## PACKAGE OUTLINE



| ABSOLUTE MAXIMUM RATING | | | |
|---|---|---|---|
| **Symbol** | **Parameter** | **Value** | **Units** |
| $P_{PP}$ | Peak Pulse Power (8/20μs) | 60 | W |
| $V_{ESD}$ | ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | ±25<br>±20 | kV |
| $T_{OPT}$ | Operating Temperature | -55/+125 | °C |
| $T_{STG}$ | Storage Temperature | -55/+150 | °C |

| ELECTRICAL CHARACTERISTICS (Tamb=25°C) | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Condition** | **Min** | **Typ** | **Max** | **Units** |
| $V_{RWM}$ | Reverse Working Voltage | Any I/O pin to GND | | | 5.0 | V |
| $V_{BR}$ | Reverse Breakdown Voltage | $I_T$ = 1mA<br>Any I/O pin to GND | 6.0 | | 9.0 | V |
| $I_R$ | Reverse Leakage Current | $V_{RWM}$ = 5V<br>Any I/O pin to GND | | | 1.0 | μA |
| $V_C$ | Clamping Voltage | $I_{PP}$ = 1A, $t_p$ = 8/20μs<br>Any I/O pin to GND | | | 10 | V |
| | | $I_{PP}$ = 4A, $t_p$ = 8/20μs<br>Any I/O pin to GND | | | 15 | V |
| | | $I_{PP}$ = 8A, $t_p$ = 8/20μs<br>Vcc pin to GND | | | 15 | V |
| $C_{ESD}$ | Parasitic Capacitance | $V_R$ = 0V, f = 1MHz<br>Between I/O and I/O | | 0.20 | 0.30 | pF |
| | | $V_R$ = 0V, f = 1MHz<br>Between I/O and GND | | 0.45 | 0.50 | pF |
| | | $V_R$ = 0V, f = 1MHz<br>Between Vcc and GND | | 0.80 | | pF |

Note: I/O Pins are pin 1,3,4,6. Pin 5 is Vcc. Pin 2 is GND.

## ELECTRICAL CHARACTERISTICS CURVE

Fig 1 Power Derating Curve

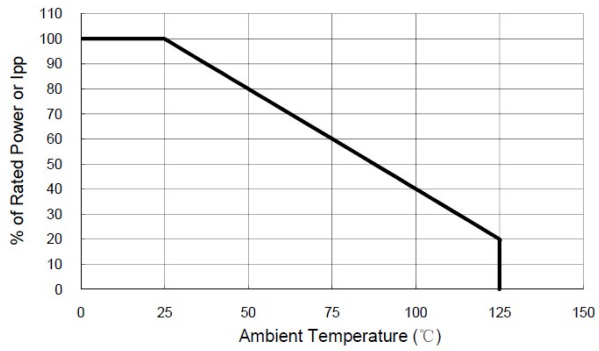



Fig 2 Clamping Voltage vs Peak Pulse Current

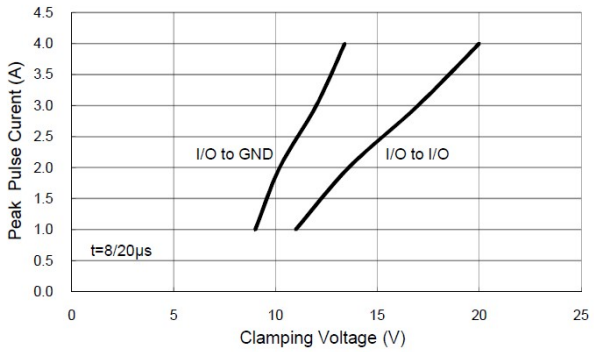



Fig 3 Voltage Sweeping of I/O to I/O

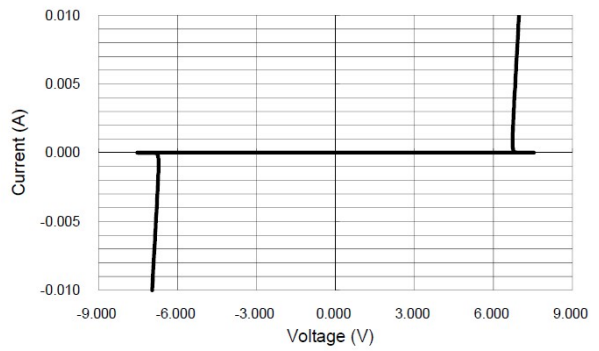



Fig 4 Voltage vs Capacitance

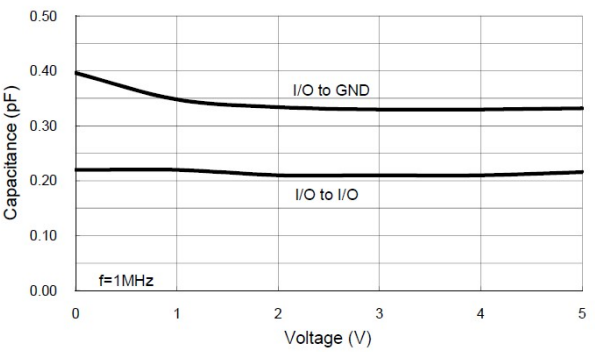



Fig 5 ESD Clamping of I/O to GND
(+8kV Contact per IEC 61000-4-2)

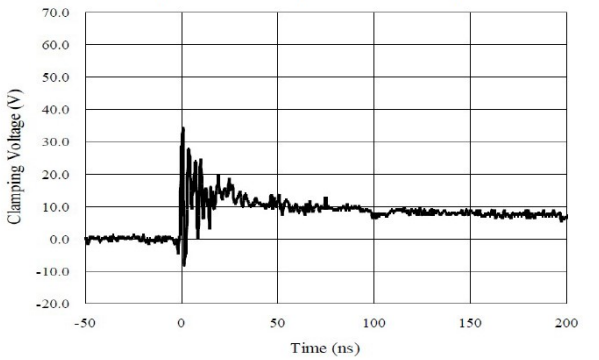
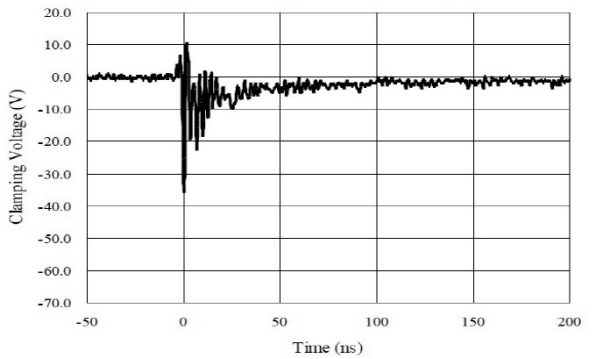
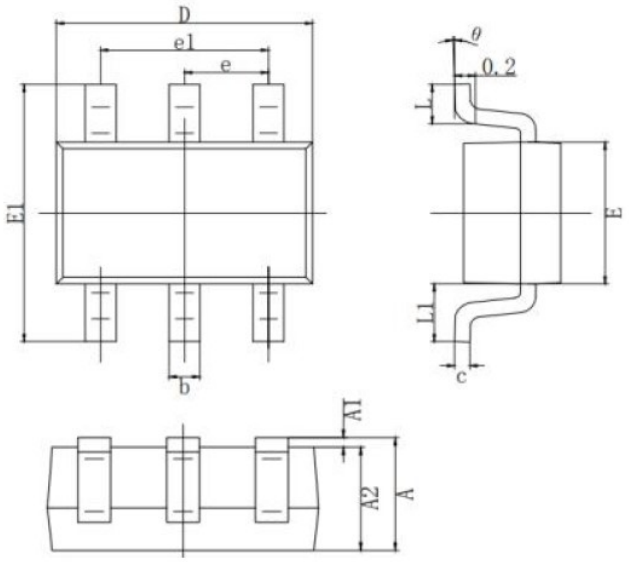



Fig 6 ESD Clamping of I/O to GND
(-8kV Contact per IEC 61000-4-2)

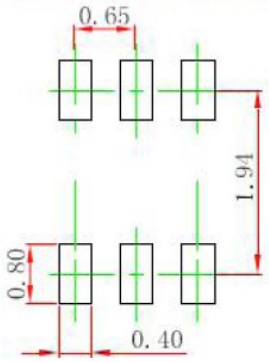


## SOT-363 PACKAGE OUTLINE DIMENSIONS




| SYMBOL | MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.900 | 1.100 |
| A1 | 0.000 | 0.100 |
| A2 | 0.900 | 1.000 |
| b | 0.150 | 0.350 |
| c | 0.080 | 0.150 |
| D | 2.000 | 2.200 |
| E | 1.150 | 1.350 |
| E1 | 2.150 | 2.450 |
| e | 0.650 TYP. | |
| e1 | 1.200 | 1.400 |
| L | 0.525 REF. | |
| L1 | 0.260 | 0.460 |
| θ | 0° | 8° |

Recommended land dimensions for SOT-363. Electrode patterns for PCBs




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.